REMARKS

Applicant respectfully traverses and requests reconsideration.

Claims 21, 2, 8-10, 23, 25-28 and 31-33 stand rejected under 35 U.S.C. §102(e) as being anticipated by Wada. Wada is directed to a computer graphics apparatus utilizing cash memory that utilizes a CPU to process image data and the cache memory retains a partial copy of the image data of the main memory. The main memory stores the image data and a video cache memory acquires image data from the main memory and the cache memory. The graphics controller acquires image data from the video cache memory and outputs the image data to the raster scan display. Wada also states: "There is no need additionally to incorporate a specialized pixel buffer for accommodating such data as the pixel color intensities." (See column 2, lines 38-40). Each graphics controller actually communicates with main memory, along with the cache memory to output image data. (See column 2, lines 49-50). As such, Wada teaches a completely different structure in at least that the main memory must be used and is used to store the video that is commonly available to the different graphics controllers. As such, the main memory, as described in Wada, is not a separate video memory for each of the graphics controllers as required by the claim.

As to claim 21, for example, the cited portion of Wada, namely FIG. 11 and corresponding description, and refers to the item 1 main memory as being the claimed first and second video memory that are each respectively associated with a different video graphics adapter. However, Applicant respectfully submits that the main memory 1 shown in FIG. 11 is as stated a "main memory" whereas Applicant claims "video memory" and as shown and described in Applicant's Specification is not main memory. An example of main memory is shown, for example, in Applicant's Specification in FIG. 4 as 414. Wada fails to teach or suggest, among other things, storing the first portion of the active video in a video memory associated with the first VGA and storing a second portion of the active video in a

video memory associated with the VGA for the second VGA. The main memory in Wada is not the claimed video memory. Accordingly, the claims are in condition for allowance.

As to claims 8 and 31, the office action alleges that FIG. 11 allegedly teaches a graphics controller 9a as a primary controller and graphics controller 9b as a secondary controller. However, Applicant respectfully challenges this interpretation as the Applicant is unable to find where, for example, in column 13, or elsewhere related to FIG. 11, that states such operation. In fact, it appears that the Wada reference would not want to have a primary or secondary graphics controller as they are all coupled to the main memory. In any event, if the rejection is maintained, Applicant respectfully requests a showing as to where this claimed subject matter is taught in the cited reference as Applicant is unable to find this discussion in the reference.

As to claims 9 and 32, Applicant respectfully reasserts the relevant remarks made above with respect to claims 8 and 31. Accordingly, these claims are also in condition for allowance.

As to claim 23, Applicant respectfully reasserts the relevant remarks made above with respect to claim 21 as again the office action alleges that main memory 1 corresponds to the claimed first and second video memories. However, as noted above, it appears that Wada actually teaches not to use separate video memories in order to reduce storage requirements and instead uses main memory for all graphics controllers. Accordingly, Wada teaches a different system and apparatus. Accordingly, the claim is in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter. For example, Applicant respectfully notes that claim 27 requires that the window operates in conjunction with an operating system such that the operating system supports a program for providing the active video data only to the first VGA yet in claim 23 that a second VGA is able to output a portion of active video data from the same frame as the first VGA. The cited

portion of Wada (namely item 6a) is silent as to any such operating system and combined operation of VGAs and video memories as claimed. As such, if the rejection is maintained, Applicant respectfully requests a showing of the claimed subject matter.

Claims 21 and 11 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hong. The Hong reference is directed to an apparatus for processing multiple types of graphics data for display wherein a first graphics controller chip is coupled to the video capture port of a second graphics controller chip. In a first mode of operation, the first chip may generate graphics pixel data for display in a first environment. The pixel data is stored in the memory of the second chip reserved for graphics pixel data and transmitted to a display device coupled to the second chip. In another mode, the video capture port of the second chip may be coupled to a video source so that the data captured in the video port is stored in the memory of the chip reserved for video pixel data. The second chip may then process and output both video pixel and graphics pixel data. As shown in Hong, the video capture port 30 of the second chip 15 receives the output from the first graphics controller chip 32. This is a different structure and operation from that claimed.

For example, the office action alleges that item 15 is the claimed "first video adapter". If this logic is kept consistent with the Hong disclosure, then Hong does not anticipate Applicant's claimed invention. For example, Applicant claims, among other things, rendering at least a second portion of the first frame of video wherein the first frame of video is received by the first video graphics adapter. If graphics adapter 15 is the "first video adapter" and receives a first frame, Hong does not teach that graphics processor 32 (the alleged second graphics processor) renders a portion received of the same frame from graphics processor 15. To the contrary, Hong teaches that the first graphics processor 15 actually receives graphics data from the second graphics controller chip 32. As such, among other things, there is no rendering of a second portion of the first frame of video in the second

graphics controller chip 32 taught in Hong in response to a second control signal and storing that in the video memory associated with graphics processing engine 15 since it is the graphics output of first graphics controller chip 32 that is passed to the graphics processor 15. There is no video information coming from the graphics processor 15 to the graphics processor 32 as taught by Hong. Accordingly, these claims are in condition for allowance.

The dependent claims are also allowable.

Claims 22 and 17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Knox et al. The Knox reference is directed to a multi-tile video display system with a single controller that does not provide standard video signals to each of the monitors. Instead, only the changed portion of an image to be displayed are sent to the monitors, which internally maintain a video frame buffer in the monitors for displaying using a displaying engine. Preferably, a high-speed serial link is used between the monitors and the video controller for transmitting this information. The Knox reference describes the use of two video graphics adapters but the secondary graphics adapter only provides 3D rendering and no video processing. In fact, the secondary card 102 does not provide the displaying of a portion of the first frame of video at the secondary VGA in response to a control signal. The cited portion refers to graphic data and not to the displaying of a first frame of active video by the secondary card. It appears that the secondary card does not display active video. The secondary card in fact only appears to render and provide graphics data and not active video. Accordingly, the claims are in condition for allowance.

Claims 6-7 and 29-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wada in further view of Dennison et al. Applicant respectfully reassert the relevant remarks made above with respect to Wada and as such, these claims are also in condition for allowance.

In addition, Applicant has added new claim 35 which describes the nature of the local and non-local bus structure noted, for example, in FIG. 3 of Applicant's Specification and elsewhere. The claimed structure does not appear to be taught or suggested by the cited references. Accordingly, Applicant respectfully submits that this claim is also in condition for allowance.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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